WHAT IS CLAIMED IS:

1. A MOSgated semiconductor device having a minimized figure of merit; said device comprising:

a die of monocrystaline silicon having a body region and an upper junction receiving layer of one conductivity type;

a plurality of elongated spaced and parallel base stripe diffusions of the other conductivity type formed in the upper surface of said junction receiving layer and a plurality of elongated source diffusions of the one conductivity type in and extending coextensively with said base stripe diffusions to define invertible channel regions along the sides of each of said elongated base stripe diffusions;

a plurality of gate stripes each comprising gate oxide stripes covered by conductive polysilicon stripes; said plurality of gate stripes overlying respective spaced pairs of adjacent invertable channel regions and the space between their respective base diffusions; said polysilicon stripes each having a width in the range of about 3.2 microns to 3.5 microns and a spacing in the range of about 1.0 to 4.0 microns;

adjacent ones of said base diffusions being spaced apart by greater then about 0.8 micron.

2. The device of claim 1 wherein said polysilicon stripes have a width of about 3.1 microns and a spacing of about 1.5 microns.

3. The device of claim 1 wherein said base diffusion have a depth of about 1.25 microns and said source diffusions have a depth of about 0.4 microns.

4. The device of claim 2 wherein said base diffusion have a depth of about 1.25 microns and said source diffusions have a depth of about 0.4 microns.

5. The device of claim 1 which further includes a plurality of second base diffusions of the other conductivity type which are centered on respective ones of said base diffusions and which have a higher concentration then that of said base diffusions and which have a lateral extent defined by the spacing of said polysilicon stripes.

6. The device of claim 2 which further includes a plurality of second base diffusions of the other conductivity type which are centered on respective ones of said base diffusions and which have a higher concentration then that of said base diffusions and which have a lateral extent defined by the spacing of said polysilicon stripes.

7. The device of claim 3 which further includes a plurality of second base diffusions of the other conductivity type which are centered on respective ones of said base diffusions and which have a higher concentration then that of said base diffusions and which have a lateral extent defined by the spacing of said polysilicon stripes.

8. A MOSgated semiconductor device having a minimized figure of merit; said device comprising:

a die of monocrystaline silicon having a body region and an upper junction receiving layer of one conductivity type;

a plurality of elongated spaced and parallel base stripe diffusions of the other conductivity type formed in the upper surface of said junction receiving layer and a plurality of elongated source diffusions of the one conductivity type in and extending coextensively with said base stripe diffusions to define invertible channel regions along the sides of each of said elongated base stripe diffusions;

a plurality of gate stripes each comprising gate oxide stripes covered by conductive polysilicon stripes; said plurality of gate stripes overlying respective spaced pairs of adjacent invertable channel regions and the space between their respective base diffusions;

a plurality of second base diffusions of the other conductivity type which are centered on respective ones of said base diffusions and which have a higher concentration then that of said base diffusions and which have a lateral extent defined by the spacing of said polysilicon stripes.

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9. The process of manufacture of a MOSgated device comprising the steps of forming a gate oxide layer atop a silicon surface of one conductivity type; forming a layer of polysilicon atop said gate oxide layer; etching said polysilicon layer and the said underlying gate oxide layer into a plurality of spaced stripes of oxide and polysilicon overlying said oxide; implanting and diffusing a plurality of spaced first base diffusion stripes of the other conductivity type into said silicon surface, using said stripes of

polysilicon as a mask; implanting and diffusing a plurality of source diffusions into said first base diffusion stripes, using said stripes of polysilicon as a mask, and leaving invertible channel regions along the outer edges of said first base diffusion stripes; diffusing third base diffusion stripes, into said silicon surface, using said stripes of polysilicon as a mask, to a depth about equal to that of said first diffusions and a width substantially equal to the space between the opposite edges of adjacent pairs of said polysilicon stripes.

10. The process of claim 9, wherein said polysilicon stripes have a width of about 3.1 microns and a spacing of about 1.25 microns.

11. The process of claim 9 wherein said first base diffusions have a depth of about 0.4 microns and said second base diffusions have a depth of about 1.25 microns.

12. The process of claim 10 wherein said first base diffusions have a depth of about 0.4 microns and said second base diffusions have a depth of about 1.25 microns.

13. The process of claim 9 which further includes the formation of insulation spacer layers over the type and edges of said polysilicon stripes and the etching of shallow openings through central portions of said source regions and into said first base diffusions; and thereafter depositing a metal layer over the upper surface of said device to contact said source regions and said first and second base diffusions.

14. The process of claim 12 which further includes the formation of insulation spacer layers over the type and edges of said polysilicon stripes and the etching of shallow openings through central portions of said source regions and into said first base diffusions; and thereafter depositing a metal layer over the upper surface of said device to contact said source regions and said first and second base diffusions.

15. A d-c to d-c converter circuit which includes a high frequency control MOSFET connected in series with a d-c source, an inductor and a d-c output and a synchronous rectifier MOSFET connected in closed circuit relation with said inductor and said d-c output; each of said control MOSFET and synchronous rectifier MOSFET being made with identical planar parallel stripe topologies but having different die areas; said synchronous rectifier area MOSFET having a die area which is greater than that of said control MOSFET.

16. The circuit of claim 15 wherein said identical topologies for each of said control MOSFET and synchronous rectifier MOSFET comprises, for each die:

a die of monocrystaline silicon having a body region and an upper junction receiving layer of one conductivity type;

a plurality of elongated spaced and parallel base stripe diffusions of the other conductivity type formed in the upper surface of said junction receiving layer and a plurality of elongated source diffusions of the one conductivity in and extending coextensively with said base stripe diffusions to

define invertible channel regions along the sides of each of said elongated base stripe diffusions;

a plurality of gate stripes each comprising gate oxide stripes covered by conductive polysilicon stripes; said plurality of gate stripes overlying respective spaced pairs of adjacent invertable channel regions and the space between their respective base diffusions; said polysilicon stripes each having a width in the range of about 3.2 microns to 3.5 microns and a spacing in the range of about 1.0 to 4.0 microns;

adjacent ones of said base diffusions being spaced apart by greater then about 0.8 micron.

17. The circuit of claim 16, wherein said polysilicon stripes have a width of about 3.1 microns and a spacing of about 1.5 microns.

18. The circuit of claim 17, wherein said base diffusion have a depth of about 1.25 microns and said source diffusions have a depth of about 0.4 microns.

19. The circuit of claim 16 which further includes a plurality second base diffusions of the other conductivity type which are centered on respective ones of said base diffusions and which have a higher concentration then that of said base diffusions and a depth which is greater than that of said base diffusions and which has a lateral extent defined by the spacing of said polysilicon stripes.

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LOW VOLTAGE MOSFET AND PROCESS FOR ITS MANUFACTURE AND CIRCUIT APPLICATION

A power MOSFET die with a minimized figure of merit has of a planar stripe MOSFET geometry in which parallel diffused bases (or channels) are formed by implantation and diffusion of impurities through parallel elongated and spaced polysilicon stripes wherein the polysilicon line width is from about 3.2 to 3.4 microns, preferably 3.4 microns; the polyline spacing is from about 1 to 4 microns, preferably 1.5 microns and the diffused bases are spaced by greater than about 0.8 microns. The polysilicon stripes act as masks to the sequential formation of first base stripes, the source stripes and second higher concentration base stripes which are deeper than the first base stripes. Insulation side wall spacers are used to define a contact etch for the source contact. The above design geometry is used for both the forward control MOSFET and the synchronous rectifier MOSFET of a buck converter circuit.